Design Technology Co-optimization in the Era of Sub-resolution Ic Scaling (Tutorial Texts)

Lars W. Liebmann, Kaushik Vaidyanathan, Lawrence Pileggi

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The challenges facing the most-advanced technology nodes in the microelectronics industry can be overcome with the help of design technology co-optimization (DTCO). This mediation process aims to ensure competitive technology architecture definition while avoiding schedule or yield risks caused by unrealistically aggressive process assumptions. This Tutorial Text reviews the fundamental design objectives as well as the resulting topological constraints of a standard cell logic design flow. Cell design, placement, and routing are examined against the backdrop of ever-increasing design constraints in advanced-technology nodes.

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